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DERINGER

Semiconductor Articles Declaration

Complete this form if you have products classifiable under 8471.50, 8471.80, or 8473.30. Please refer to the Further Guidance section at the bottom of this form for specifics on technical parameters for semiconductor articles to be subject to 232 tariffs. If you ship some goods that are subject to these tariffs and some that are not, speak to your Deringer contact about supplying documentation other than this form or attach a detailed list to this form. Failure to pay duties on subject goods can result in adverse action from CBP. By signing this form, you acknowledge that you have read the entire form and understand your responsibilities as the importer of record.

Complete for Single Shipment Declarations ONLY

Description of Goods: ______________________________

Product#: ______________________________ HTSUS Number(s): 10 Digits Required

Shipment Entry No., Invoice or Reference No.: ______________________________

☐ My good(s) classifiable in 8471.50, 8471.80, or 8473.30 meet the technical parameters outlined in the Proclamation and are subject to an additional 25% duty under 9903.79.01.

☐ My good(s) classifiable in 8471.50, 8471.80, or 8473.30 either do not meet the technical parameters outlined in the Proclamation or are otherwise exempt and no additional duty is owed. Specify Chapter 99 number to enter for your goods:

______________.

Complete ONLY for Blanket Declarations

Description of Goods: ______________________________

Product#: ______________________________ HTSUS Number(s): 10 Digits Required

☐ My good(s) classifiable in 8471.50, 8471.80, or 8473.30 meet the technical parameters outlined in the Proclamation and are subject to an additional 25% duty under 9903.79.01.

☐ My good(s) classifiable in 8471.50, 8471.80, or 8473.30 either do not meet the technical parameters outlined in the Proclamation or are otherwise exempt and no additional duty is owed. Specify Chapter 99 number to enter for your goods:

Annual Certificate Period, covering from ______________ to ______________

I hereby certify that the previous statements regarding my products are true and correct to the best of my knowledge.

Company Name: ______________________________ Account Number: ______________

Address: ______________________________

City, State/Province, and Zip/Postal Code: ______________________________

Name of Certifying Individual: ______________________________ Title: ______________

Phone No.: ______________________________ Email: ______________

Signature: ______________________________ Date: ______________

Further Guidance

Per Presidential Proclamation, "Adjusting Imports of Semiconductors, Semiconductor Manufacturing Equipment, and Their Derivative Products into the United States," effective January 15, 2026, certain semiconductor articles are subject to a 25% 232 duty. In order for an article to be subject to the tariff, it must be classifiable in 8471.50, 8471.80, or 8473.30, must be a logic integrated circuit, or an article that contains a logic integrated circuit **AND** meet the following technical parameters:

(1) a total processing performance (TPP) greater than 14,000 and less than 17,500, and a total DRAM bandwidth greater than 4,500 GB/s and less than 5,000 GB/s; **OR**

(2) (2) a total processing performance greater than 20,800 and less than 21,100, and total DRAM bandwidth greater than 5,800 GB/s and less than 6,200 GB/s.

For the purposes of this note, total processing performance (TPP) is 2 × "MacTOPS" × "bit length of the operation," aggregated over all processing units on the integrated circuit. "MacTOPS" is the theoretical peak number of Tera (1012) operations per second for multiply-accumulate computation (D = A × B + C). The 2 in the TPP formula is based on the industry convention of counting one multiply-accumulate computation (D = A × B + C) as two operations for purpose of product datasheets. Therefore, 2 × "MacTOPS" may correspond to the reported TOPS or FLOPS on a product datasheet. The "bit length of the operation" for a multiply-accumulate computation is the largest bit-length of the inputs to the multiply operation. The TPP for the imported product is determined by aggregating the TPP for each processing unit on the integrated circuit: TPP = TPP1 + TPP2 + … + TPPn (where n is the number of processing units on the integrated circuit). The rate of "MacTOPS" is to be calculated at its maximum value theoretically possible. The rate of "MacTOPS" is assumed to be the highest value the manufacturer claims in annual or brochure for the integrated circuit. For example, a "TPP" threshold of 4800 can be met with 600 tera integer operations (or 2 × 300 "MacTOPS") at 8 bits or 300 tera FLOPS (or 2 × 150 "MacTOPS") at 16 bits. If the integrated circuit is designed for MAC computation with multiple bit lengths that achieve different "TPP" values, the highest "TPP" value should be used. For integrated circuits that provide processing of both sparse and dense matrices, the "TPP" values are the values for processing of dense matrices (e.g., without sparsity).

For the purposes of this note, "total DRAM bandwidth" refers to the aggregate memory bandwidth in gigabytes per second between the integrated circuit (IC) and dynamic random access memory (DRAM) ICs, including copackaged DRAM ICs and non-copackaged DRAM ICs. Copackaged DRAM ICs include, for example, high bandwidth memory (HBM). Non-copackaged DRAM ICs include, for example, graphics double data rate (GDDR) ICs. "Total DRAM bandwidth" does not include bandwidth from DRAM ICs accessed remotely over an interconnect medium.

Additionally, these **duties do not apply** in the following scenarios:

- 9903.79.02: Semiconductor articles that are classifiable under provisions of the HTSUS subject to HTSUS 9903.79.01 but that do not meet the required technical parameters.
- 9903.79.03: Semiconductor articles that are for use in U.S. data centers. A "U.S. data center" refers to a facility that requires greater than 100 megawatts (MW) of new load dedicated to AI inference, training, simulation, or synthetic data generation.
- 9903.79.04: Semiconductor articles that are for repairs or replacement in the United States.
- 9903.79.05: Semiconductor articles that are for research and development in the United States. "Research and development" is defined as any activity that is (a) a systematic, intensive study directed toward greater knowledge or understanding of the subject studied; (b) a systematic study directed specifically toward applying new knowledge to meet a recognized need; or (c) a systematic application of knowledge toward the production of useful materials, devices, services or methods, and includes design, development and improvement of prototypes and new processes to meet specific requirements.
- 9903.79.06: Semiconductor articles, that are for use by startups in the United States. A "startup" is an "emerging growth company," as defined at 15 U.S.C. § 77b(a)(19).
- 9903.79.07: Semiconductor articles that are for use in non-data center consumer electronics applications in the United States, including gaming, personal computing, professional visualization, workstation applications, and automotive applications.
- 9903.79.08: Semiconductor articles that are for use in non-data center civil industrial applications in the United States, including factory robotics and industrial machinery.
- 9903.79.09: Semiconductor articles that are for use in United States public sector applications.